Notice of References Cited

Application/Control No.

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Examiner

Vuthe Siek

Applicant(s)/Patent Under
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TEIG ET AL.

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			·
	В	US-			
	С	US-			
	D	US-			
	E	US-			
	F	US-			
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	1	US-			
	J	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					0
	Р					
	Q					
	R					
	s					
	Т					

NON-PATENT DOCUMENTS

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)					
	U	DEGUCHI et al., "TIMING-DRIVEN HIERARCHICAL GLOBAL ROUTING WITH WIRE-SIZING AND BUFFER-INSERTION FOR VLSI WITH MULTI-ROUTING-LAYER," IEEE, Jan 28, 2000, pp. 99-104.				
	v	Das et al., "CHANNEL ROUTING IN MANHATTAN-DIAGONAL MODEL," IEEE, JAN 1996, PP. 43-48.				
	w					
	х					

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.